808 Gilman Street Berkeley, CA., 94710 p:925.253.2960 www.furaxa.com

SAMPULSE20x2 DUAL PULSER/SAMPLER DEMO BOARD

USER MANUAL 12/27/15

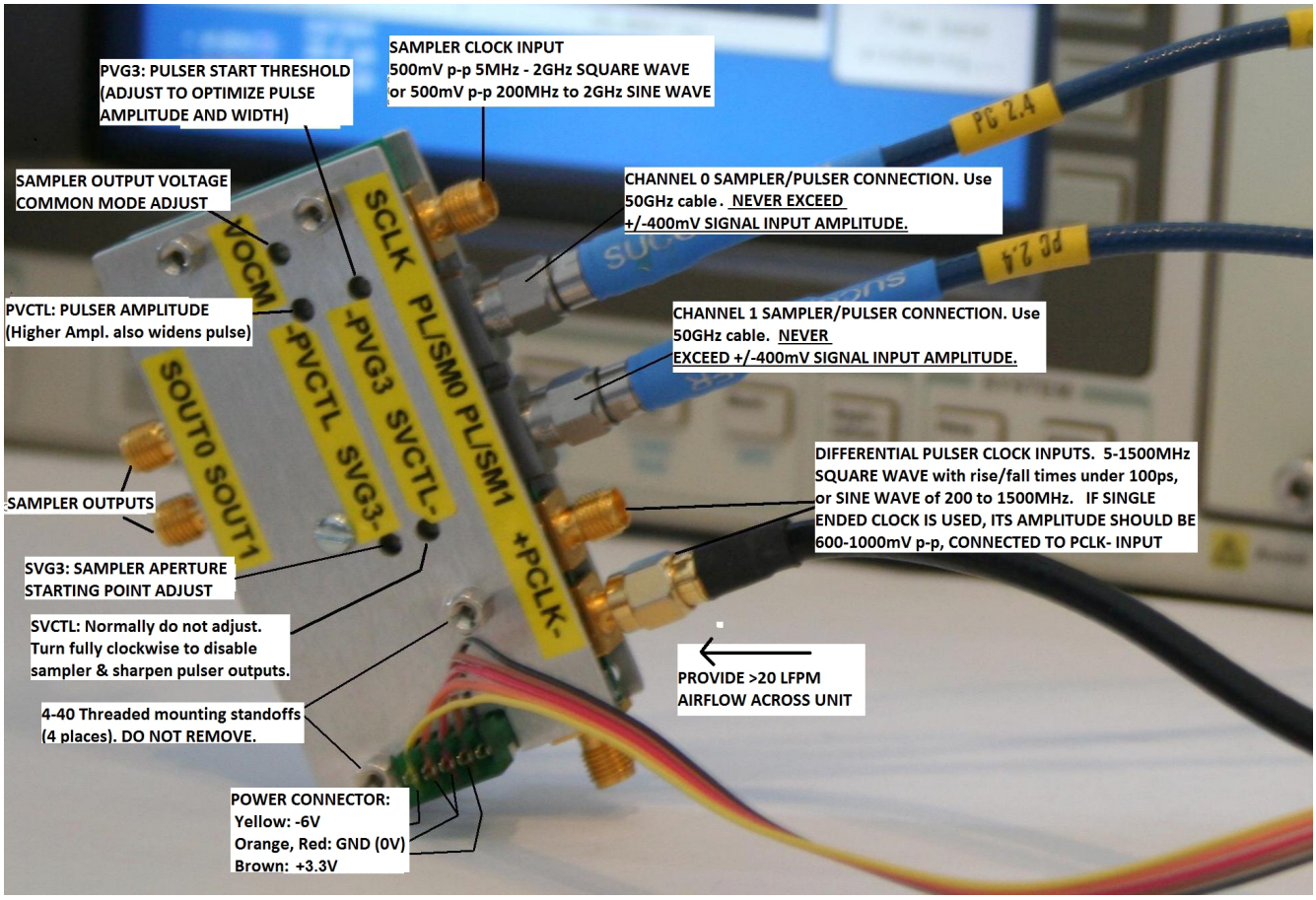

Figure 1. Connections to SAMPULSE20x2 demo board. **DO NOT UNSCREW SPACERS ON EITHER SIDE OF UNIT. APPLY ONLY LIGHT FINGER TORQUE TO CONNECTORS**.

INTRODUCTION:

The SAMPULSE20x2 is a demonstration board for the Furaxa SiGe3 30GHz sampler/pulser IC. The SIGe3 IC is a dual channel sampler pulser chip, and the SAMPULSE20x2 demonstration board contains two 2.4mm combined TDR input/output connectors (ESMA connectors may alternatively be specified at time of order), one to each sampler/pulser channel in the IC. The SiGe3 IC's two sampler outputs are then sent to to two SMA jacks, the first outputting the sample taken on the rising edge of the sampler clock, and the second containing the sample taken on the falling edge of the sampler clock.

The sampler clock input, which must be a square wave with rise time under 150pS, may be set to any frequency from 5 MHz to 2GHz, causing the board take two pairs of samples (one on each clock edge) at rates from 5 million to 2 billion per second. A sine wave input may alternatively be used, but it must be at least 200MHz to ensure acceptable jitter. Amplitude must be between 500mV p-p and 1V p-p.

A pulser clock input, which may be set to any frequency from 5 MHz to 2GHz and must be a square wave (preferably differential) with rise time under 150pS, causes the board to produce concurrent pulses on both of the SiGe3's I/O pins, producing near-concurrent pulses at the two sampler/pulser TDR input/output connectors.

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SAMPLER SPECIFICATIONS:

Sample rate: 5MSPS to 2000MSPS (clock sources under 200MHz must be square wave)
Number of channels: 2
Full Scale Input range: +/- 200mV – **DO NOT EXCEED +/- 400mV.**
3dB Input Bandwidth: 10 GHz
6dB Input Bandwidth: 19 GHz
Usable Bandwidth while maintaining 40dB SNR: 50 GHz (with 2.4mm connector option, 26GHz with SMA option)
Dynamic Range: 85dB typical, 5MHz to 20 GHz.
SFDR: 40dB at maximum input level
Input connector type: 2.4MM Jacks (ESMA jacks may optionally be specified)
Output connector type: Two SMA connectors:
Output signal +/- 500mV peak, with adjustable offset voltage of 0 to 2V into 50 ohms.
DO NOT ADJUST ABOVE 1V WHEN USING DC-COUPLED 50 OHM LOAD

PULSER SPECIFICATIONS:
Pulser clock inputs: Differential or single ended, AC coupled, amplitude 500mV p-p to 1000mV p-p.
Pulse repetition rate: 5MPPS to 2000MPPS (clock sources under 200MHz must be square wave with <150ps rise time – slower rise times will result in broader output pulse)
Pulse amplitude (pulser may be disabled): Adjustable from approximately 30mV to 300mV
Pulse width, at 2.4mm input/output connector: Approximately 16-22ps, viewed on HP 54750/54752A scope.

Demo Board Power Requirements:
+3.3V (+3V to +4V OK) at 210mA typ.), -6V at 150mA typ.

Cooling Requirements:
Light Fan cooling required: 20LFPM minimum.

SETUP DIRECTIONS:

1) Verify that voltages on external power supply are set to +3.3V and -6V. **Turn off external power supply**, and **connect both Orange and Red wires to grounds** (common) on external power supply. Connect **+3.3V output to brown wire** as shown in figure 1. **Connect -6V output to yellow wire**.

2) Using a high quality flexible 40 or 50 GHz microwave cable with 2.4MM connectors (or good quality 3.5mm or ESMA connectors if SMA option was specified), connect the PL/SM0 or 1 jack(s) to the desired device(s) to be driven by the SAMPULSE20x2 pulser outputs (initially the unit's operation should be verified by connecting this output to a sampling oscilloscope). **Board is fragile – do not apply excessive torque when tightening cables on connectors on the SAMPULSE20x2 (a light finger tight connection is adequate on all cable connections). 2.4MM/ESMA CONNECTORS MUST NEVER BE CONNECTED TO ANY INPUT THAT CONTAINS A VOLTAGE OF OVER +/-400mV, OR THE UNIT MAY BE DESTROYED - A FAILURE NOT COVERED BY WARRANTY.**

3) Using flexible cables, connect a square wave clock source (500 – 1000mV p-p, preferably differential) with rise time <100ps, to the PCLK + and - connectors. If you use a differential source, the + and – inputs must be out of phase by 180 degrees (with <50ps mismatch). If using a single ended source, the p-p amplitude must be between 600mV and 1000mV. For initial testing, use a sine wave or square wave, with a frequency of 500 MHz. As the output pulses are narrow (20ps) and may be difficult to find, it is most convenient to use as high a clock frequency as possible for initial testing.

4) Turn on the power supply and drive source. You should see a pulse output similar to that in figure 2.

5) To use the sampler, connect the SMA outputs to an oscilloscope, set for 10us per division, 20MHz filtering, a.c. Coupling, 50 ohm input impedance and a vertical scale of 100mV per division.

6) Using a flexible SMA cable, connect Connect a stable 0.5V p-p square wave with rise time under 2ns, or 400mV RMS sine wave, clock source to the SCLK connector. The frequency chosen should be approximately 20 KHz lower than that of the pulser clock discussed above.

7) Connect a terminator to the 2.4mm or ESMA sampler/pulser jack(s). You should see a pulse with some ringing on the oscilloscope, as shown in figure 4. Please refer to section "USING THE SAMPLER" for more details. **IMPORTANT: The samplers have been adjusted at the factory for optimal operation at 500 MSPS. When using different sampling clock frequencies (input to SCLK), you may need to adjust the SVCNTL potentiometer slightly for optimal linearity and bandwidth.**

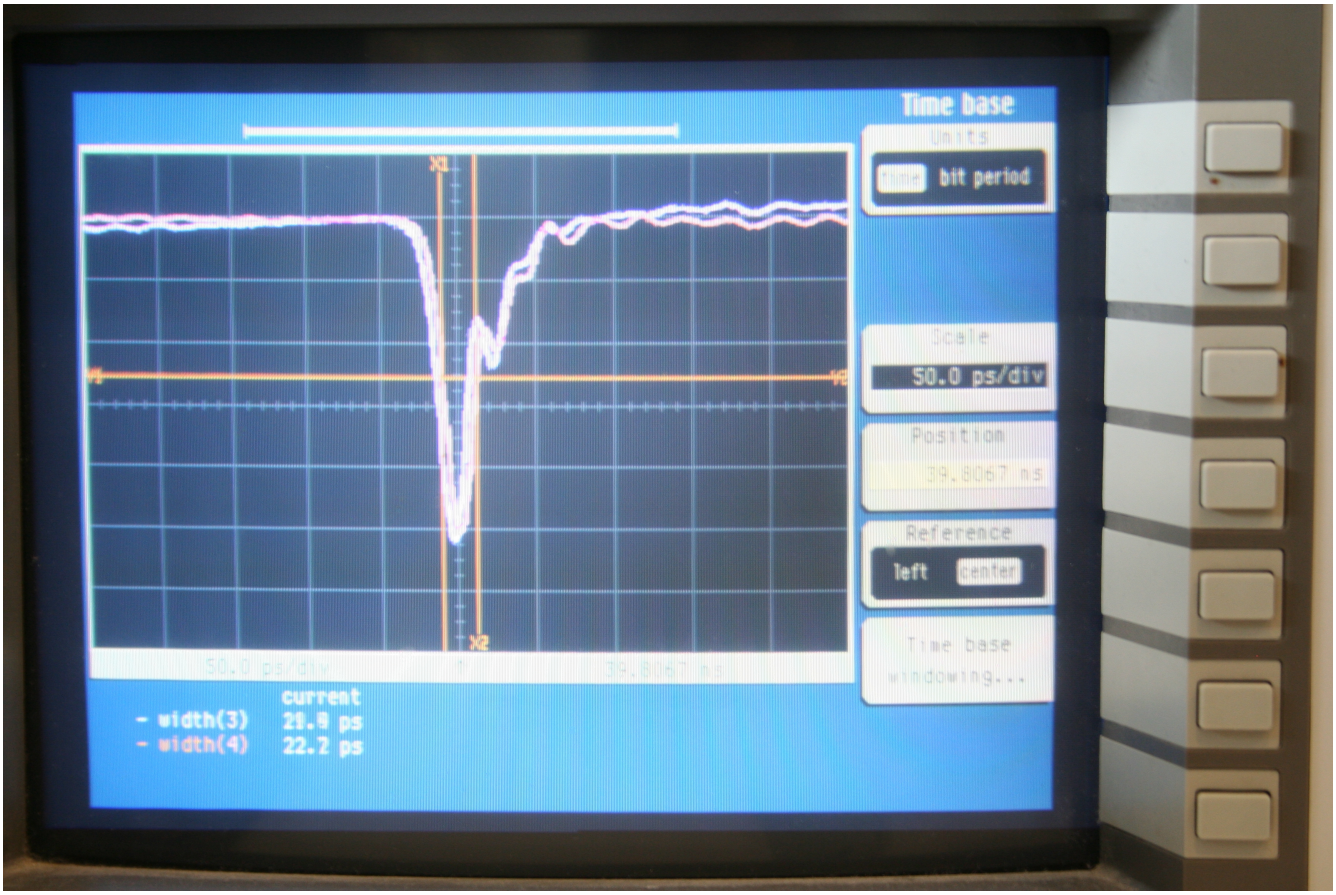

Figure 2. Expected pulse output waveforms (250mV peak on each of the two outputs) from SAMPULSE20x2, with factory setting of pulse shape (and sampler not disabled), connected to sampling scope through two 40 GHz cables. If you do not see pulse when testing unit, do not make adjustments to pulser. Instead, verify clock source waveform, cabling and connections, and power supply voltages. If external clock source is suspect, initially test pulser by connecting 1000 MHz 600mV RMS sine wave to PCLK- input.

Adjusting Pulse Amplitude (Optional)

Once basic operation and correct setup of unit, have been verified, and you are seeing a waveform similar to that shown in Figure 2, you may optionally set the unit for increased pulse amplitude (at the expense of increased pulse width) if needed. Normally, this should not be necessary, and should only be done if the pulse amplitude or width is insufficient for your application. If this adjustment is needed, use a quality alignment screwdriver, with plastic handle and metal end-blade. Insert it straight in and perpendicular to the metal plate (as shown in Figure 4), to avoid the end-blade from shorting the circuitry surrounding the adjustment potentiometer. Gradually rotate the screwdriver until it engages with the slot in the potentiometer, and view the shape of the pulse as it is adjusted, using a sampling oscilloscope. **Incorrect adjustment may make the pulse disappear, so adjustment should only be done while the existing pulse is visible on an oscilloscope or other display device, and should be done only if absolutely necessary.**

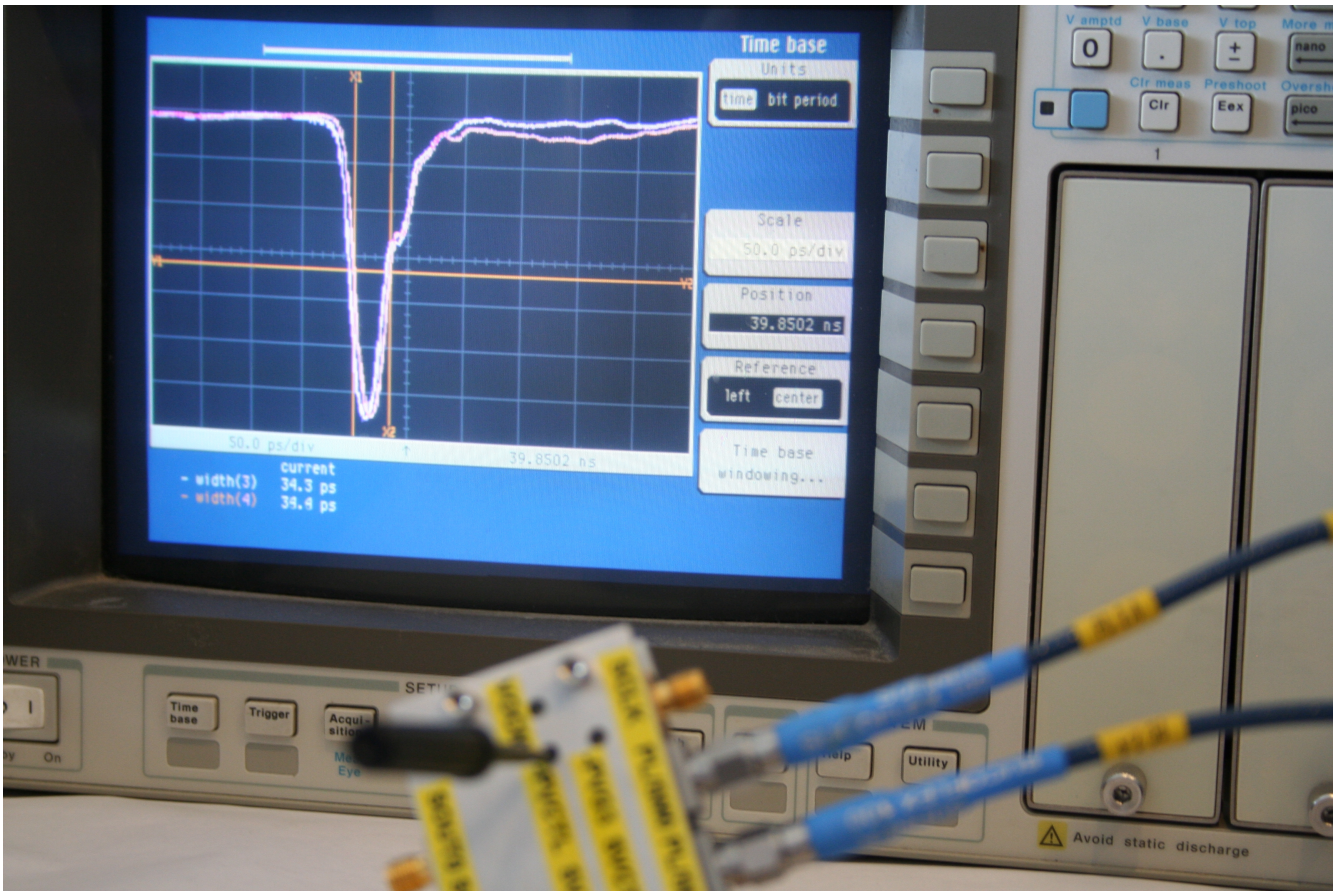

Figure 3. Optionally Adjusting PVCTL potentiometer to increase pulse Amplitude, using alignment screwdriver (blurred black object shown above) for 320mV, 35ps-wide pulses. Adjustment should be attempted only if additional amplitude is needed. Pulse PVG3 potentiometer may be further adjusted if needed to optimize pulse amplitude and width.

USING THE SAMPLER.

The IC that generates the pulse inside the SAMPULSE20x2 also has two samplers that can take 15ps snapshots of the generated pulse and its reflections from the device being driven, as well as any external signals fed into the 2.4mm or ESMA jacks. To use the sampler(s), connect to the Sampler Clock Input a continuous square wave having a frequency that differs from that of the continuous pulser clock (PCLK) input by approximately 2KHz to 100KHz. The two sampler outputs may then be fed into a low-pass filter with a cutoff frequency of approximately 25MHz, and then viewed by an A/D converter or on a low-speed oscilloscope or ADC board (with approximately 20 MHz bandwidth limiting filter). The waveform so displayed will be the heterodyned (downconverted) picture of the pulse and its reflections, as shown in figure 5. Note that in this figure, the two sampler outputs show the downconverted pulse train at different times (despite the fact that the pulses on the two channels are virtually concurrent), as one sampler channel samples its input waveform on the rising edge of SCLK and the other channel samples its input waveform on the falling edge of SCLK.

IMPORTANT: The samplers have been adjusted at the factory for optimal operation at 500 MSPS. When using different sampling clock frequencies (input to SCLK), you may need to adjust the SVCNTL potentiometer slightly for optimal linearity and bandwidth.

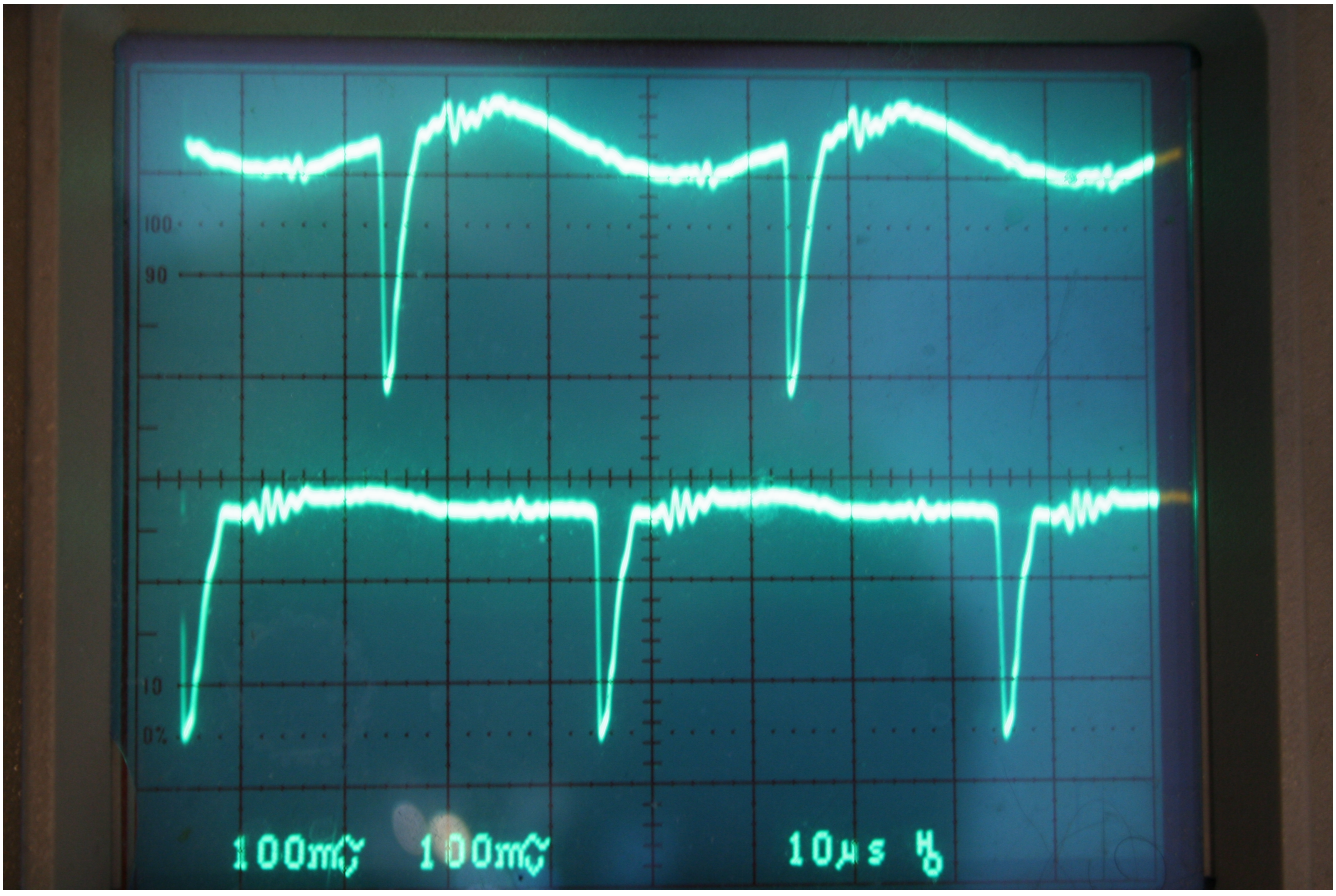

Figure 4. Sampler outputs (two differential halves) showing heterodyne of pulse train of pulses spaced 2ns apart (990.025 MPPS), generated by on-chip pulser. Sampler is run at 990 MSPS, resulting in 25,000 waveforms/second (40 microseconds of scope display corresponds to ~1ns of real time).

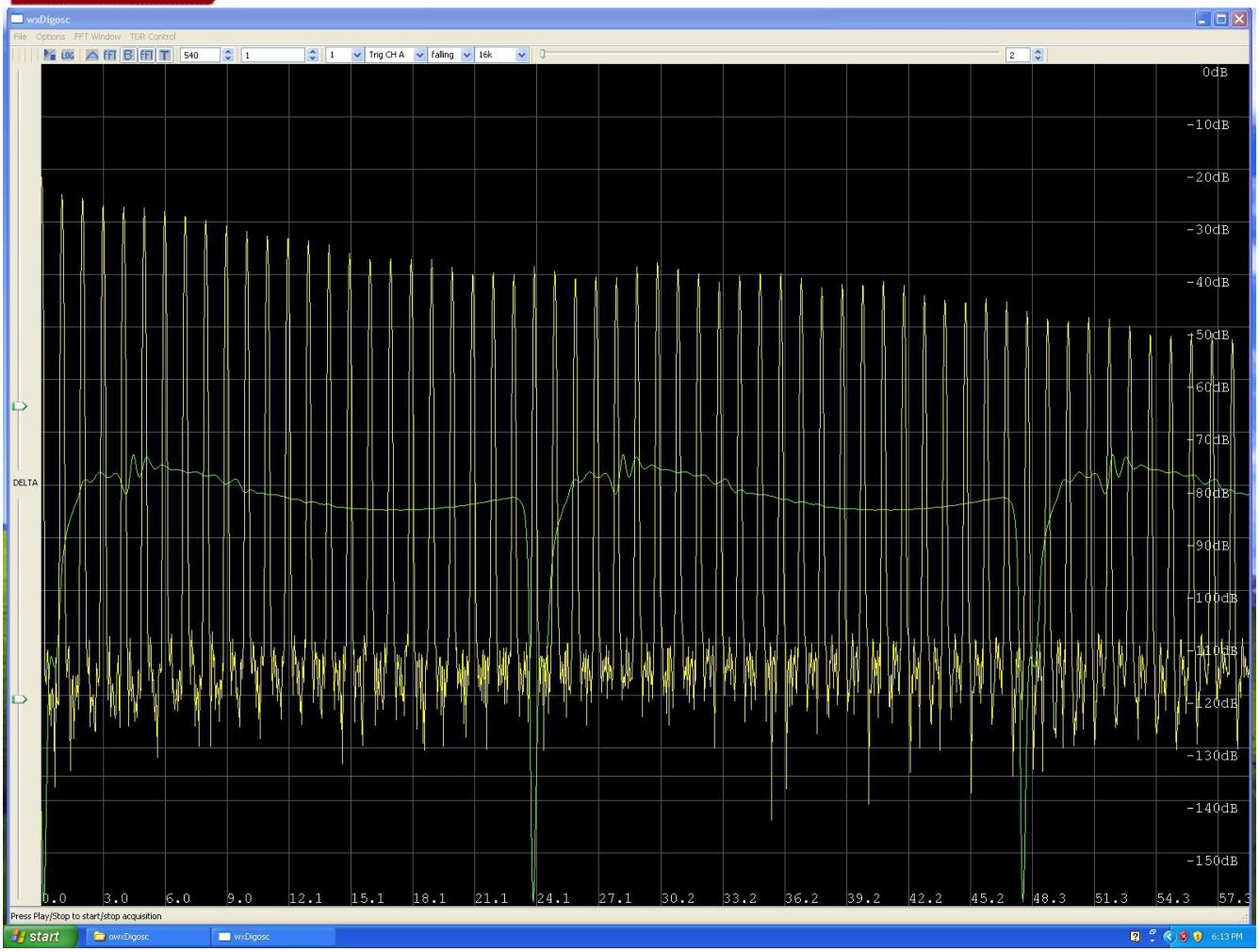

Figure 5. Sampler output viewed on Ultraview AD16-250x4 ADC board, showing heterodyne of train of pulses spaced 1.0101 ns apart (990.025MPPS), generated by on-chip pulser. Sampler is run at 990MSPS, resulting in 25,000 waveforms/second (40 microseconds of sampler output display corresponds to 1.0101ns of real time). Green trace is time domain display, yellow is frequency spectrum. Each comb tooth corresponds to a multiple of 990MHz contained in the pulse train. Zeroeth tooth at very left of window is DC, second tooth is 990MHz component, third is 1.980GHz, fourth is 2.97GHz, … last is 28.71 GHz. Combined frequency rolloff shown is due to roll-off of pulser energy multiplied by rolloff of sampler frequency response. At 9 GHz, sampler response is 3dB down from low frequency peaks, and pulser energy content is down 3dB, resulting in total depression of 6dB from low frequency response. At approximately 47 GHz, combined response is down 20dB, meaning that sampler and pulser response are each down by about 10dB from low frequency performance. Sampler response, and pulser energy combs are both usable to over 50GHz.

Optionally Defeating the Sampler, so as to Improve the Shape of the Generated Pulse.

Figure 6 is a photo showing how the pulse may be sharpened up (at the expense of the samplers being disabled), by adjusting the SVCTL potentiometer fully clockwise. The screw should be turned slowly clockwise as shown in Figure 6, while observing the resulting signal, for an optimal pulse width. A small reduction in amplitude, as well as a DC offset will result, but this DC may be blocked by subsequent circuitry after the pulser. Figure 6 shows the resulting improved pulse shape, as well as the adjustment screwdriver in the correct hole for this adjustment. The sharper pulse may also result in more ringing.

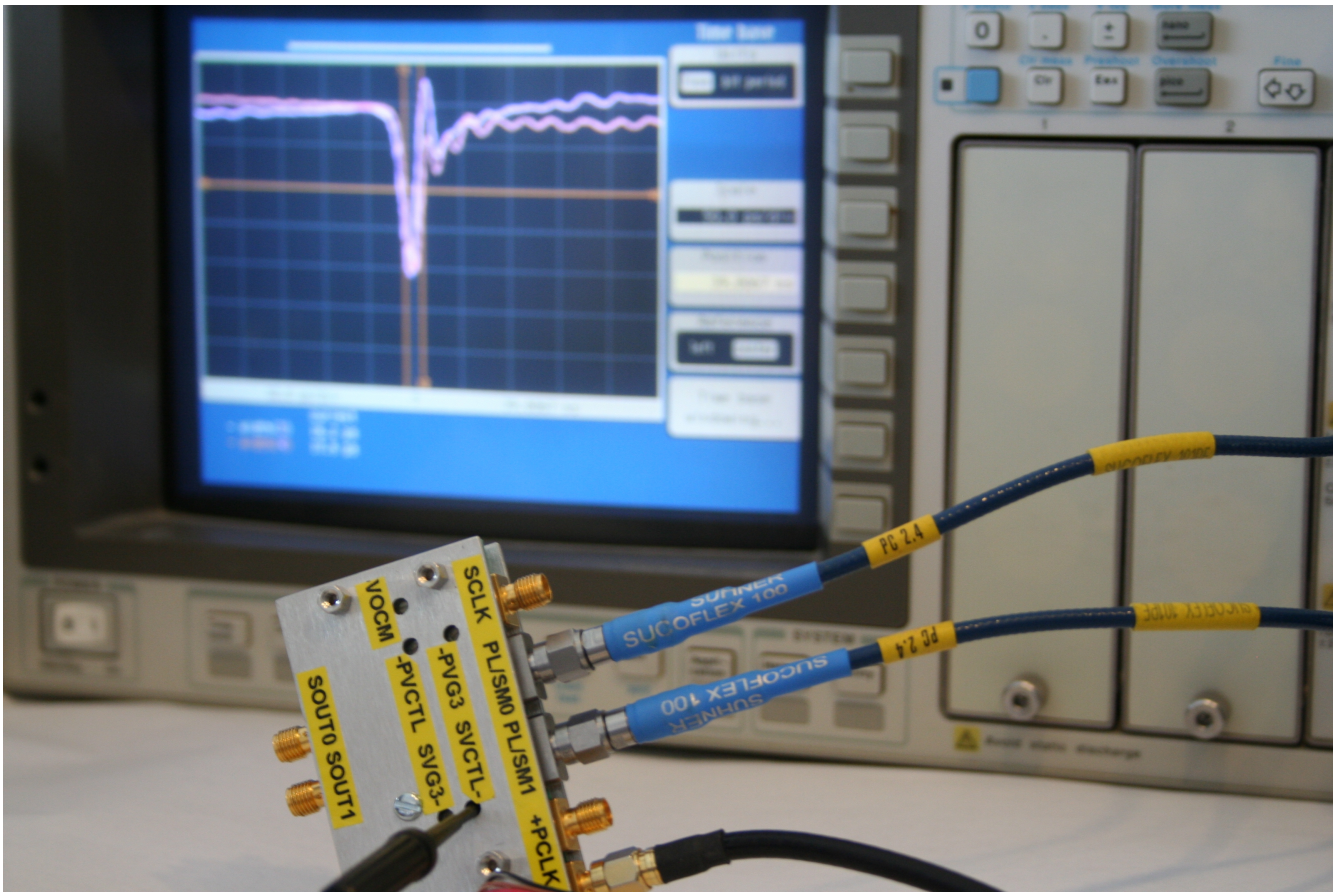

Figure 6. Faster pulse shape due to sampler being disabled, by turning SVCTL potentiometer fully clockwise. Note black adjustment screwdriver in the correct hole for adjustment. Vertical scale is 50mV / division. Pulse widths are under 18ps, although two pulser outputs vary as to degree of ringing and baseline shift.

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Appendix: Noise, Distortion and Crosstalk Characterization for Sampulse20

Measurement Setup:

A 500MHz, +6dBm amplitude, sampling clock is input to the SCLK input of the Sampulse20, resulting in each of the two channels sampling at 500 MSPS. One channel samples on the positive edge of this clock, while the second channel samples on the negative edge.

Sampler Noise Floor Measurement:

Initially, to measure the noise floor of the SAMPULSE20, no inputs were connected to the SAMPULSE20's sampler input channels (which are internally resistively terminated), and a a Rohde and Schwarz FSP-38 microwave spectrum analyzer was used to measure the output spectrum of each output channel in sequence. The noise floor was measured at approximately -88dB below the maximum output level of -5dBM, resulting in an **estimated dynamic range of 83dB over the SAMPULSE20's IF bandwidth of 400MHz**.

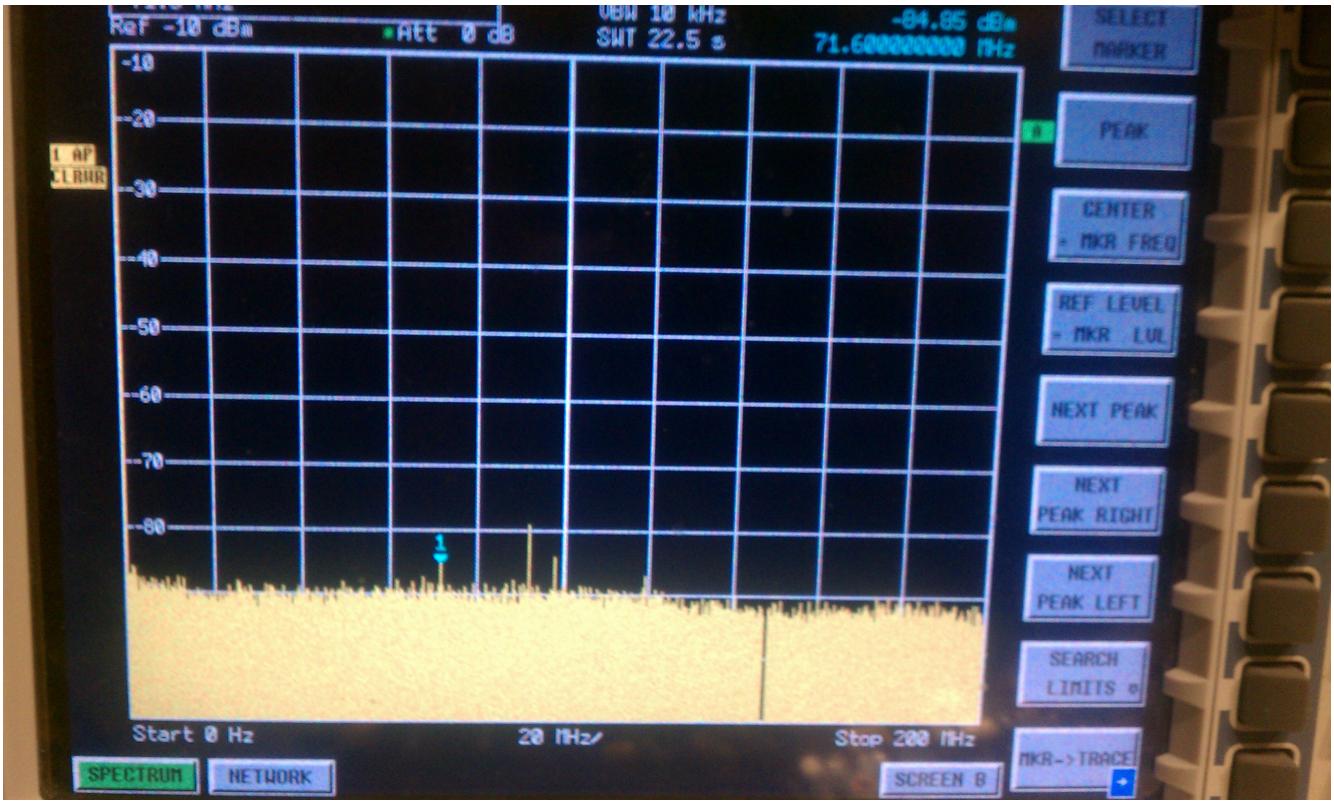

Figure 1. Noise floor of SAMPULS20 over 9KHz to 200MHz output frequency range.

Distortion and Crosstalk Measurements:

Test signals of -25dBm and -10dBm (maximum input level), generated by a Hittite HMC-T2100 microwave signal generator, were input to the first of the two sampler input channels, while the other input was left unconnected. The outputs of both channels was observed using a Rohde and Schwarz FSP-38 microwave spectrum analyzer. Test frequencies of 100MHz, 1100MHz, 2100MHz, 3100MHz, ….. 18,100MHz, 19,100MHz, resulting in a sampled output (IF) of 100MHz in all cases. Figure 2 below shows a representative distortion measurement, in this case with an input frequency of 12.1GHz (100MHz offset from 24th harmonic of 500M-SPS sampling rate).

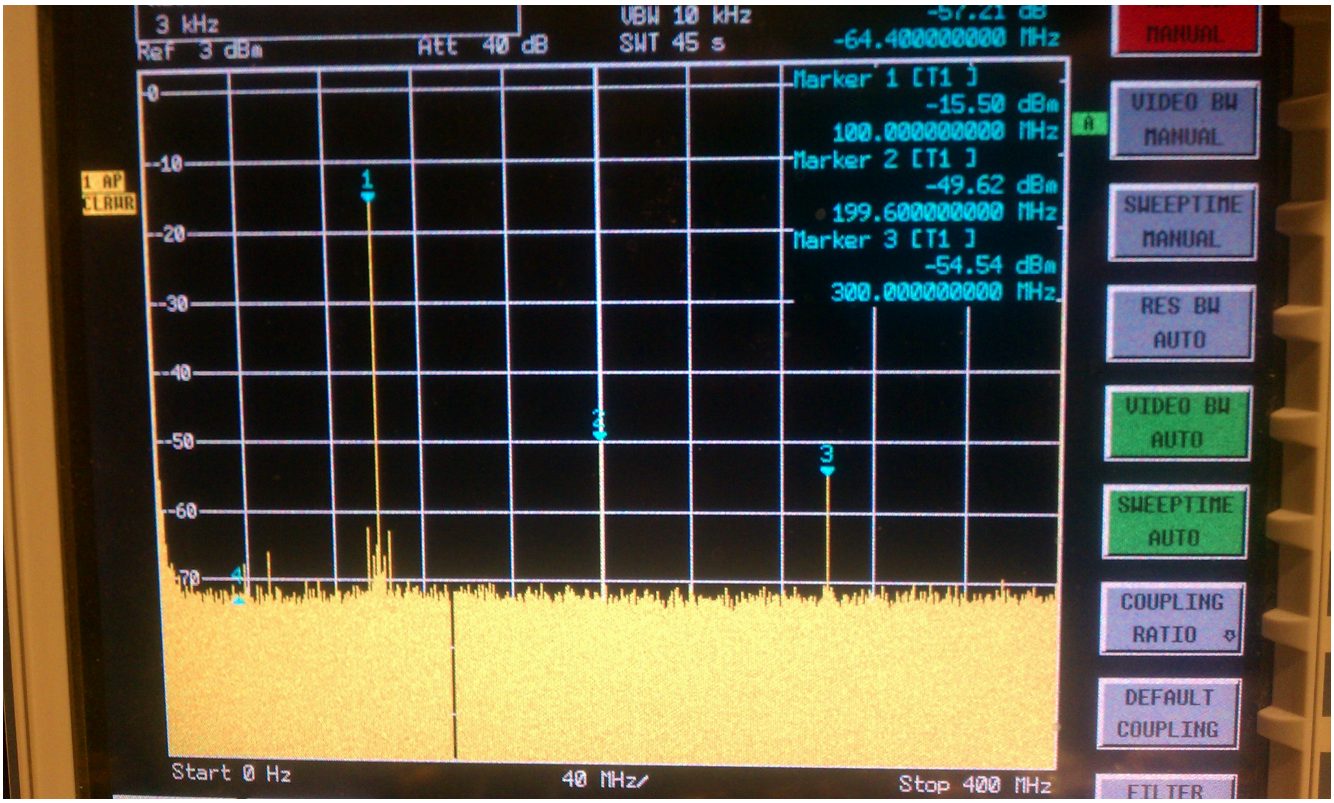

Figure 2. Distortion measurement at 12.1GHz input at -10dBM input level. Main IF output (Marker 1) of 100MHz (= 12.1GHz – 24x500MHz), at -15.5dBm. Second harmonic distortion component (Marker 2) is at -49.6dBM (-34.1dBc). Third harmonic distortion component (Marker 3) is at -54.54 (-39dBc).

Crosstalk measurements were then made by continuing to drive the first input channel with a -10dBm signal while measuring, with the spectrum analyzer, the output of the second channel, whose input was not driven. Figure 3 below shows the output of the second channel, showing crosstalk of -43.3dB for an input frequency of 12.1GHz.

Table 1 below shows frequency response, 2nd harmonic distortion (HD2), 3rd harmonic distortion (HD3) and crosstalk, for a range of input frequencies from 100MHz to 19.1GHz, for an input level of -10dBM (full scale). Table 2 below shows the same information, but for an input level of -25dBM.

Figure 3. Crosstalk measurement at 12.1GHz input at -10dBM input level. Main IF output (Marker 1) of 100MHz (= 12.1GHz – 24x500MHz), at -58.8dBm, which indicates a crosstalk value of -43.3dB at that input frequency.

Frequency: (GHz)	Output Level (100MHz IF,dBm)	HD2 (dBc)	HD3 (dBc)	Crosstalk (dBc)
0.1	-7	-28	-26	-65
1.1	-7.4	-26.6	-33.6	-54.6
2.1	-8	-29	-34	-60
4.1	-9	-32	-38	-43
6.1	-11	-39	-42	-56
8.1	-12	-38	-41	-37
10.1	-14	-36	-39	-34
12.1	-15.5	-34.5	-38.5	-43.3
14.1	-16	-32	-38	-30
16.1	-17	-35	-40	-33
18.1	-20	-32	-37	-31
19.1	-21	-36	-39	-42

Table 1. HD2, HD3 and Crosstalk, for input signals of -10dBm (near maximum) at various frequencies. HD2 and HD3 are computed by subtracting second and third harmonic peaks, respectively, from level of main 100MHz IF peak.

Frequency: Output Level HD2 HD3 Crosstalk
(GHz) (100MHz IF,dBm) (dBc) (dBc) (dBc)
0.1 -18 -38 -40 -67
1.1 -19 -48 -54 -54.6
2.1 -20 -49 -53 -60
4.1 -21 -48 -54 -43
6.1 -24 -47 -61 -56
8.1 -25 -47 -57 -37
10.1 -27 -45 -55 -35
12.1 -30 -46 -54 -43
14.1 -30 -44 -53 -32
16.1 -31 -42 -48 -34
18.1 -32 -44 -50 -34
19.1 -33 -45 -51 -45

Table 2. HD2, HD3 and Crosstalk, for input signals of -25dBm (approximately 1/4 of full-scale input) at various frequencies. HD2 and HD3 are computed by subtracting second and third harmonic peaks, respectively, from level of main 100MHz IF peak.

Summary

Crosstalk varies from -65dBc at low input frequencies, to -30dBc at 14.1 GHz when driven by a full scale input. Crosstalk improves by about 2dB (to -67dBc at 100MHz and -32dBc at 14.1GHz) when input level is reduced to approximately ¼ of full scale.

Second harmonic distortion (HD2) varies from -26.6dBc at an input frequency of 1.1GHz to -39dBc at 6.1GHz, for a full scale input. HD2 improves to a worst case value of -38dBc at 0.1GHz and -45dBc at 19.1Ghz when reducing input level to approximately ¼ of full scale.

Third harmonic distortion (HD3) varies from -26.dBc at an input frequency of 0.1GHz to -42dBc at 6.1GHz, for a full scale input. HD3 improves to -40dBc at 0.1GHz and -51dBc at 19.1Ghz when reducing input level to approximately ¼ of full scale.